converting means for converting said graphic data temporarily stored in said storage into serial data which is supplied to output means, said output means outputs graphic data read out from said memory.

64. A memory controller according to claim 63, wherein said successive groups of m bits of data from said m bit terminals are read out of said memory by performing plural read operations within a memory cycle based on an address specified by said processor.

65. A memory controller according to claim 64, wherein said n bits of data is applied to said processor through said n bit terminals in a unit of time more than two times said memory cycle.

66. A memory controller according to claim 63, wherein said successive groups of m bits of data each includes an m bit portion of said n bits of data. --

REMARKS

In paragraphs 1 through 4 of the Office Action the Examiner objected to the Reissue Declaration as being defective under 35 USC §251 and 37 CFR §1.175. A new Reissue Declaration is now being prepared and will be filed as soon as executed. The new Reissue Declaration will address the objections raised by the Examiner in paragraphs 1-4. However, it should be noted that claims 1-12, 14, 16,

and 18-34 were cancelled. Therefore, the objections raised by the Examiner with respect to these claims are rendered moot. Particularly, the Examiner's objection to claims 21, 22, 28-34 and 42 as not being directed to the invention disclosed in the original application as set forth in paragraph 5 of the Office Action and the objection to claims 10, 12 and 22 as allegedly being an attempt to recapture cancelled subject matter as set forth in paragraph 7 of the Office Action are rendered moot.

However, with respect to the rejection of claims 14, 18, 19, 24, 25, 28-34, 36, 37, 39, 42, 43, 47 and 48 under 35 USC §251 as set forth in paragraph 6 Applicants traverse this rejection being that it appears the Examiner is substituting his own reason as to the reason for discovering the invention. The Examiner states that his reasons do not comport with the features now recited in the claims. 35 USC §251 and MPEP §1412.01 is not concerned with the reasons or objects of the invention as alleged by the Examiner but is only concerned that the reissue claims are directed to the invention as disclosed in the original application. Such is the case in the present application being that each of the features recited in the claims are clearly disclosed in the originally filed application. In the "BACKGROUND OF THE INVENTION" section of the originally filed specification Applicants clearly describe that in the conventional apparatus "although the memory is connected to a 16 bit data bus, the dynamic random access (DRAM) generally poses a one-bit or four-bit data bus and hence at least 4 to 16 memory

elements are required". The alleged minimization and reduced size is merely a goal which is accomplished by rearranging the data buses in the manner recited in the claims of the present application to allow for the interfacing of an n bit bus with an m bit bus where n is greater than m. This interfacing feature of the present invention is the structure which accomplishes the desired goal of reduced size and cost alleged by the Examiner as being the invention. Each of the now pending claims clearly recites such an interfacing feature. Therefore, the claims of the present application are clearly directed to the invention as originally disclosed in the application.

Claims 8, 9, 14, 16, 34 and 44-48 stand rejected under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention. As indicated above, claims 8, 9, 14, 16 and 34 were cancelled. Therefore, this rejection with respect to claims 8, 9, 14, 16 and 34 is rendered moot. Amendments were made to claims 44-48 to bring them into conformity with the requirements of 35 USC §112, second paragraph. Therefore, Applicants submit that this rejection is overcome and should be withdrawn.

Specifically amendments were made to claims 44-48 to overcome the objections noted by the Examiner in paragraph 8d of the Office Action.

Claims 14 and 18 stand rejected under 35 USC §112, fourth paragraph as being of improper dependent form for

failing to further limit the subject matter of a previous claim. As indicated above, claims 14 and 18 were cancelled. Therefore, this rejection is rendered moot.

Claims 4-7 stand rejected under 35 USC §102(e) as being anticipated by Lymelsky. As indicated above, claims 4-7 were cancelled. Therefore, this rejection is rendered moot.

Claims 1-3 and 8 stand rejected under 35 USC §103 as being unpatentable over Lymelsky in view of Kinoshita. As indicated above, claims 1-3 and 8 were cancelled. Therefore, this rejection is rendered moot.

Claims 9-12, 14, 16, 18-34 and 44-48 stand rejected under 35 USC §103 as being unpatentable over Graciotti. As indicated above, claims 9-12, 14, 16 and 18-34 were cancelled. Therefore, this rejection with respect to claims 9-12, 14, 16 and 18-34 is rendered moot. This rejection with respect to claims 44-48 is traversed for the following reasons. Applicants submit that the features of the present invention as now recited in claims 44-48 are not taught or suggested by Graciotti whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

As argued in the December 22, 1995 Amendment, the arguments of which are incorporated herein by reference, Graciotti fails to teach or suggest numerous features of the present invention as recited in the claims. Particularly, it was shown that Graciotti fails to teach or suggest that graphic data is being processed by a processor and is stored

in memory as recited in the claims of the present application. The Examiner acknowledges such by stating that:

> "Graciotti does not explicitly disclose that graphics data is processed."

However, the Examiner provides an unsupported statement that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Graciotti as claimed because Graciotti discloses a bus conversion system for use in a general processing system and such systems are often used to process graphics data. This statement by the Examiner is completely unsupported by Graciotti and other references of record. The Examiner is merely using hindsight, relying on the teachings of Applicants' disclosure, to allege what may be possible in Graciotti without pointing to any objective teaching in Graciotti or any of the other references of record to support the allegation. Thus, the Examiner has not made a prima facie case of obviousness with respect to this feature recited in the claims.

Further, Graciotti fails to teach or suggest the successive retrieval from memory of successive groups of m bits of data during a predetermined period of time as recited in the claims. In fact the Examiner states that:

> "Graciotti does not explicitly disclose that retrieval is within a memory cycle"

However, the Examiner provides an unsupported statement that it would have been obvious to one of ordinary skill in

the art at the time the invention was made to configure Graciotti as claimed because it is well known in the art that computer systems usually define a predetermined time for accessing memory (memory access time) and Graciotti teaches that the conversion is to be transparent, therefore, it would have been obvious to maintain the predefined memory access time of the processor as claimed. However, this allegation by the Examiner is completely unsupported by Graciotti or any objective teaching in Graciotti or any of the other references of record. In fact this allegation by the Examiner misses the point being that the present invention recites that successive groups of m bit of data are retrieved from memory. Such teaching cannot be found in Graciotti.

Still further, with respect to the now pending claims, the Examiner has not at any point addressed the feature recited in the claims regarding the converter. In the present invention the converter converts the graphic data temporarily stored in the storage into serial data which is provided to the output means. The converter recited in the now pending claims corresponds to element 2020 illustrated in Fig. 4 of the present application which is described on page 4, lines 45-51 of the present application. The converter 2020 is described as converting parallel data into serial data which represents 4 bit video signals provided to the CPLT 40 and CRT 50 illustrated in Fig. 1 of the present application. At no point in the Office Action has the

Examiner addressed these features nor are they taught or suggested by Graciotti.

Therefore, Applicants submit that the features of the present invention as recited in claims 44-48 are not taught or suggested by Graciotti whether taken individually or in combination with any of the other references of record.

New claims 49-66 were added. These claims recite the same features shown above not to be taught or suggested by Graciotti whether taken individually or in combination with any of the other references of record.

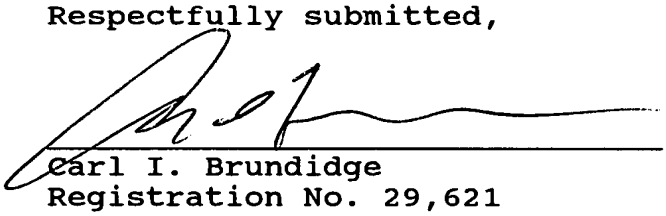
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference utilized in the rejection of the claims.

In view of the foregoing amendments and remarks, Applicants submit that claims 44-65 are in condition for allowance. Accordingly, early allowance of claims 44-65 is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 C.F.R. section 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to

Deposit Account No. 01-2135 (Case No. 500.26967R00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,



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